REMARKS

Claims 1-20 are pending. Independent claims 1, 11, and 20 were rejected under 35 U.S.C. 102(e) as being anticipated by Hum (U.S. Patent Application Publication No. 2004/0123047). The independent claims 1, 11, and 20 were also rejected under 35 U.S.C. 102(e) as being anticipated by Webb (U.S. Patent No. 6,751,721).

Hum describes "use of an import cache and/or an export directory with an agent within to respond to requests for data. The import cache stores data that has been imported through the agent. The export directory stores information related to data that has been exported through the agent. Because the import cache and the export directory only store data that has passed through the agent, not all data transferred within a system are tracked by a single import cache or export directory" (Abstract). "If the import cache returns a match, 430, the matching entry (or the relevant data from the matching entry) is retrieved from the import cache, 440. If the import cache returns a miss, indicating no match, the request for the data is sent to the nodes and/or agents represented by the agent receiving the request, 445. In one embodiment, the cache protocol state machine forwards the request to the node/agent(s) through the tracker, router and cluster interface as illustrated above with respect to FIG. 2." (Paragraph 96). "If a matching entry is retrieved, 440, the data retrieved from the matching entry is used to respond to the request. In one embodiment, the cache protocol state machine generates a response message, for example, a DataF message or a DataS message. The response message is sent through the system interface as illustrated above with respect to FIG. 2." (Paragraph 97).

Hum, however, does not describe "providing response information with a completion indicator to the processor" as recited in independent claims 1, 11, and 20. In one example, the completion indicator is a completion bit provided with response information ... If a completion bit is not provided, the requesting processor 901-3 ... expects responses from other nodes in the system. In one example, the requesting processor 901-3 expects response from nodes in the cluster of the requesting processor as well as a response from a home cluster cache coherence controller (Page 25, lines 19-28).

Hum only provides a "response message" and does not teach or suggest providing any

completion indicator to the processor. The Examiner argued that and Acknowledge message is a completion indicator. By contrast, an acknowledge message is described as a message that "indicates that the requested data has been sent to the Requesting node" (paragraph 44). The acknowledge message does not provide any completion indicator as recited in the claims. Providing a completion bit as recited in the claims allows for a variety of benefits as described in the specification of the present application.

Webb describes a "directory-based multiprocessor cache control scheme for distributing invalidate messages to change the state of shared data in a computer system. The plurality of processors are grouped into a plurality of clusters. A directory controller tracks copies of shared data sent to processors in the clusters. Upon receiving an exclusive request from a processor requesting permission to modify a shared copy of the data, the directory controller generates invalidate messages requesting that other processors sharing the same data invalidate that data." (Abstract)

Webb, however, also does not describe "providing response information with a completion indicator to the processor" as recited in independent claims 1, 11, and 20. The Examiner argues that the "completion indicator" is the number of invalid messages from processors containing the requested shared data line. However, providing responses from processors containing the requested shared data line is not a completion indicator. In fact, Webb describes a system where no completion indicator is used at all.

Dependent claims 5 and 15 further recite "wherein the completion indicator notifies the first processor that the response from the cache coherence controller will be the only response." Neither Webb nor Hum teach or suggest any completion indicator that notifies the processor that the response from the cache coherence controller will be the only response." Both Webb and Hum either wait for additional responses, timeout, or are not configured to wait for additional responses and consequently do not need any "completion indicator."

In light of the above remarks relating to independent claims and certain dependent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of

Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER/WEAVER & THOMAS, LLP

Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100